A NEW INNER LAYER SILICON STRIP DETECTOR FOR D0

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The D0 experiment at the Fermilab Tevatron is building a new inner layer detector to be installed inside the existing D0 Silicon Microstrip Tracker (D0SMT). The Layer 0 detector is based on R&D performed for the RunIIb silicon upgrade that was cancelled in the fall of 2003. Layer 0 will be installed inside the ~2.2 cm radius opening available in the D0SMT support structure with the detector in the collision hall. Layer 0 will reduce the radius of first sampling from 2.7 to 1.6 cm and substantially improve on the radiation hardness of the D0SMT, insuring that the silicon tracker remains viable through Tevatron RunII.

1. Introduction

1.1. *Physics Motivation*

The physics motivations for building a new inner layer silicon strip detector, Layer 0, are to mitigate tracking losses due to detector failures, provide more robust tracking and pattern recognition for higher luminosities, and improve impact parameter resolution. Figure 1 illustrates the increased parameter resolution by a factor of approximately two with the addition of Layer 0 for low transverse momentum particles. This translates into a 20% increase in the efficiency of tagging *b* jets and the possible resolution of B_s meson flavor oscillations.

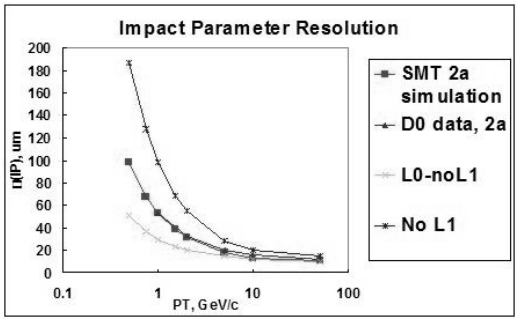

Figure 1. Impact parameter resolution with the addition of Layer 0.

1.2. *Mechanical Specifications*

Layer 0 is designed to fit inside the existing RunIIa detector and will utilize much of the existing infrastructure as well as the new electronics and readout chip designed for the cancelled RunIIb silicon replacement [1]. The current D0 Silicon Tracking detector consists of 12 disks positioned between six 4-layer barrel structures. Figure 2 shows an end view of the current detector with the new Layer 0 superimposed in the center.

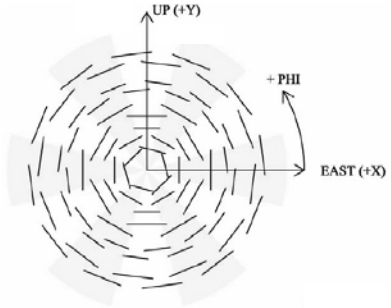

Figure 2: South End View with Layer 0 superimposed in center.

Layer 0 is designed to slide over the beryllium beam pipe and associated mounting flanges that have a diameter of 30.48 mm. The detector is also required to maintain ~1 mm separation from the beam pipe to limit capacitive coupled noise. The new detector clears the inner most layer of the current detector through a 44.04 mm diameter aperture. In addition to the tight mechanical constraints the detector is designed to maximize acceptance (98.5%) and readout segmentation. Figure 3 is an enlarged view of Layer 0 illustrating sensor positions.

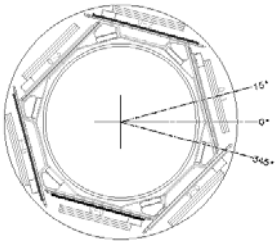

Figure 3: Layer 0 end view of sensor positions.

A 6-fold geometry was chosen with an A (inner) layer of sensors positioned at a radius of 16 mm and B (outer) layer sensors at a radius of 17.6 mm. Hybrids are located outside of the active volume and are connected to the sensors with fine pitch analog cables. Z segmentation is limited to eight sensors of 70 and

120 mm lengths by the radial buildup of the cable bundles. This arrangement provides better segmentation near Z=0 and equalizes the load capacitance by having lower sensor capacitance on the strings with longest analog cables. Table 1 summarizes the geometric dimensions of the Layer 0 components.

Table 1. Geometric parameters of the Layer 0 detector.

Layer	Radius	Z segment	Readout/ (Strip) pitch	Sensor Length	Cable Lengths
0A	16 mm	inner	71 (35.5) μm	70 mm	320, 346 mm
0A	16 mm	outer	71 (35.5) μm	120 mm	167, 244 mm
0B	17.6 mm	inner	81 (40.5) μm	70 mm	320, 346 mm
0B	17.6 mm	outer	81 (40.5) μm	120 mm	167, 244 mm

1.3. *Electronics*

Layer 0 SVX4-based instrumentation is designed to operate within the constraints of the currently installed SVX2 data acquisition system. Newly designed components consist of silicon sensors, pitch adapters, analog cables, hybrids, digital jumper cables, junction cards, twisted pair cables, and adapter cards.

1.3.1. *Sensors, pitch adapters*

Layer 0 is composed of 48 silicon sensors manufactured by Hamamatsu. Inner radius positions utilize 71μm pitch sensors while 81μm pitch sensors are used at larger radius positions. Both sensor types have intermediate strips that are not read out. A single cable pitch is accomplished by utilizing ceramic pitch adapters mounted on the sensors that also carry decoupling capacitors.

1.3.2. *Analog Cables*

Analog cables provide an interface between the pitch adapters and the SVX hybrids. To minimize mass in the active region, 91 μm pitch kapton cables are used. The analog cables are flexible circuits manufactured by Dyconex. The cable lengths vary, with the longest at 34.6 mm, and have a capacitance of .35 pF/cm. Careful design of these cables was required to minimize the capacitance presented to the SVX4 preamplifier. Kapton mesh spacers with ~90% open area are used to separate analog cables thus minimizing capacitive coupling. The

signal/noise is roughly equal at each Z location with adequate signal available for tracks incident at the extreme edges of the detector for reliable readout and reconstruction.

1.3.3. *SVX4, hybrids, digital jumper cables, twisted pair, adapter card*

The SVX4 chip is a 0.25 μm technology silicon readout chip originally developed for the RunIIb upgrades [2]. These chips use a protocol similar to the currently installed SVX2 chips but operate with a single 2.5V supply rather than the 3.3–5V supplies needed for the SVX2. Each ceramic BeO hybrids hold two SVX4 chips. Grounding of the SVX4 reference to the support structure is through vias plated through the hybrid to contacts on the co-cured flex circuit on the supports.

Digital signals from the hybrid are carried to the end of the support structure using a kapton flex digital jumper cable. The jumper cable is then coupled to a twisted pair cable using a junction card located on the existing silicon support structure. An adapter card with active circuitry, mounted on the wall of the D0 calorimeter, interfaces Layer 0 to the existing readout.

1.3.4. *Grounding and Isolation Techniques*

A number of RunIIb studies have established that low coherent noise can be achieved by good low inductance ground connections to the support structure [3]. This is accomplished by co-curing mesh ground planes onto the carbon fiber support structure and utilizing low inductance flex circuits which carry bias and ground from the bottom to the top of the sensors.

Since Layer 0 is a longitudinally continuous conductor, the potential exists for a serious ground loop encircling the D0 calorimeter. The adapter card was designed to provide electrical isolation from D0. This card converts single ended SVX2 control signals, supplied by existing electronics, into differential signals needed by the SVX4. Utilizing the high impedance of the differential signals ground isolation is achieved. In addition, a separate isolated 2.5 Volt supply provides power to the SVX4 chips. The isolation requirement is greater than 10 Ohms.

2. Performance

2.1. *Mechanical Measurements*

The completed Layer 0 detector mechanical dimensions have been compared to aperture measurements of the RunIIa silicon detector taken during an access in 2004. The aperture measurements show that Layer 0, with an outer radius of 22.02 mm will have a radial clearance to the existing structures by .86 mm horizontally and 1.67 mm vertically. The 1mm spacing requirement, to prevent capacitive noise coupling from the beam pipe, has also been insured.

2.2. *Grounding and Isolation*

Two noise issues arose while testing Layer 0. The isolated low voltage power supply for the SVX4 chips was found to require a filter to reduce pick-up noise on the readout. Five turns of the power cables on a ferrite core reduced the noise to acceptable levels. A LC filter has been design and is ready for testing.

The resistive temperature device (RTD) system also caused noise on the readout. The RTD system consists of a RTD soldered onto a flex circuit affixed longitudinally to Layer 0. The flex circuit is then adapted to cryogenic type wire. A braided shield around the cryogenic wire connected to the Layer 0 isolated ground eliminated the noise.

2.3. *Signal to Noise Response*

Maximizing the signal to noise response has been addressed throughout the design of Layer 0. With a single minimum ionizing particle equivalent to ~ 30 ADC counts, readout test show that a 16:1 noise ratio has been attained with a 200V sensor bias and a ferrite core on the isolated power supply leads.

3. Conclusion

A new inner layer silicon detector has been designed, built, and tested for the D0 experiment. Strict mechanical specifications, electrical isolation from D0, and a high signal to noise ratio have been demonstrated. Layer 0 will be installed during the next shutdown period scheduled for early 2006.

Acknowledgments

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References

1. D0 Collaboration, “D0 Layer 0 Conceptual Design report,” (2003).
2. L. Christofek, *et al*., “SVX4 User’s Manual”, D0 Note 004251 (2003).
3. K. Hanagaki, *Nucl. Inst. And Meth.Phys.* **A511**, 121 (2003).